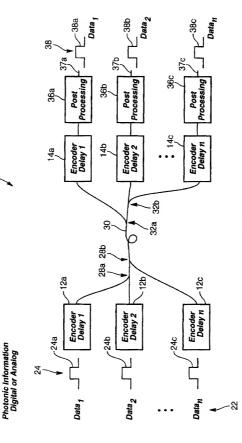
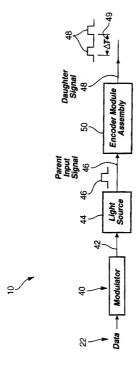


FIG. 1 2807.2.4.10

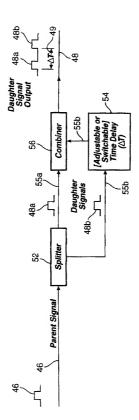


**Fig. 2** 2807.2.4.10



Differential Delay Multiplexer Sender/Encoder

**Fig. 3** 2807.2.4.10



Differential Delay Multiplexer (DDM) Sender/Encoder

Fig. 4 2807.2.4.

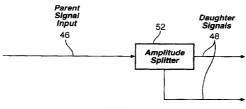
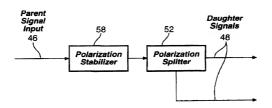
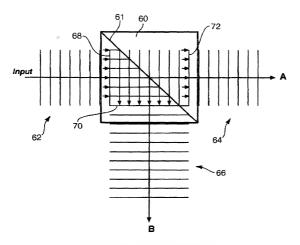


FIG. 5



**Splitting Criteria** 

FIG. 6



**Amplitude or Polarization Splitter** 

FIG. 7 2807.2.4.

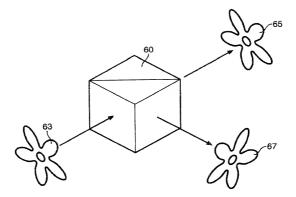
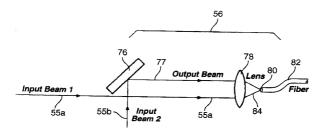


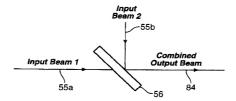
Image Signals Which Maintain Spatial Information

FIG. 7A

2807.2.4.

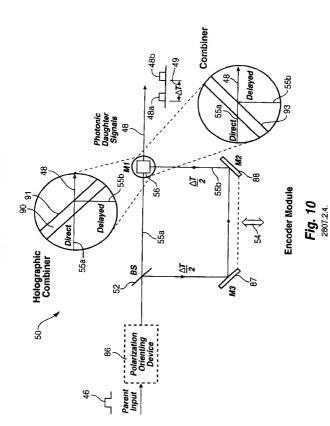


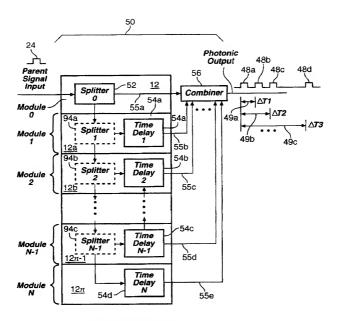
**Beam Combiner** FIG. 8



# **Amplitude or Polarization Combiner**

FIG. 9 2807.2.4.





Composite Encoder Module Assembly

FIG. 11 2807.2.4.

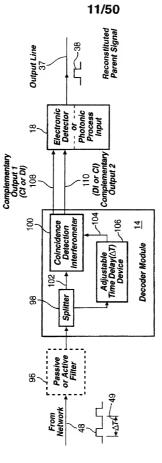


Fig. 12

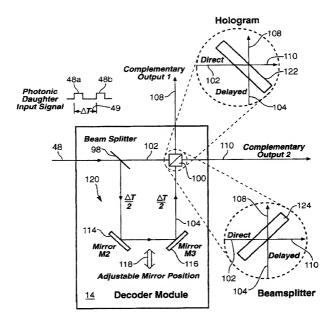


FIG. 13

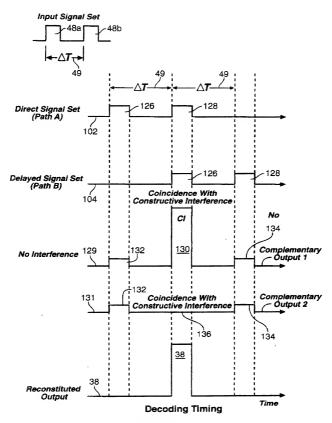


FIG. 14

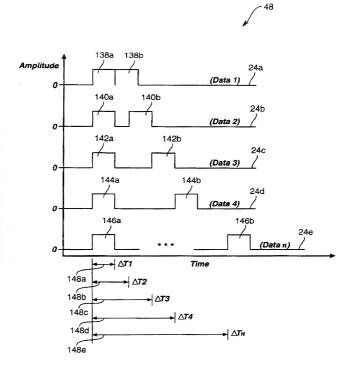


Fig. 15

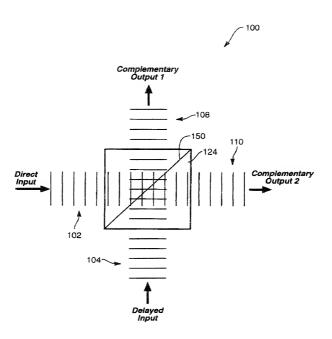


Fig. 16

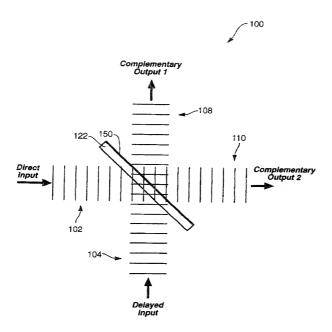


Fig. 17

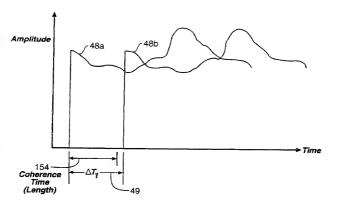


Fig. 18

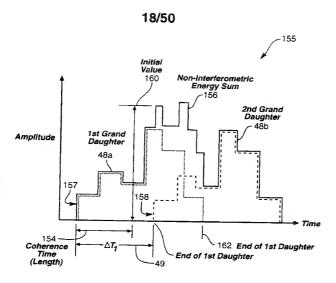


Fig. 19

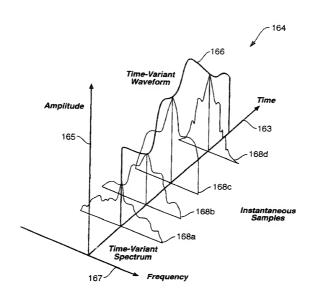


Fig. 20

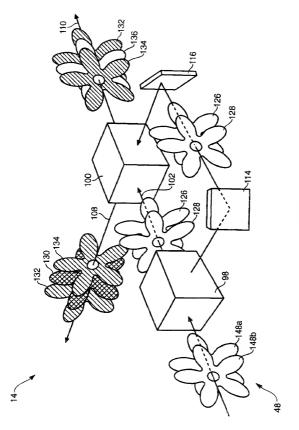
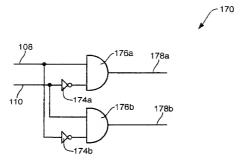
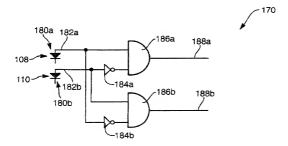


Fig. 21

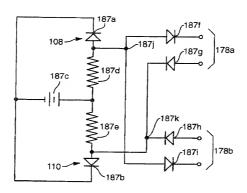


Photonic Processor Fig. 22



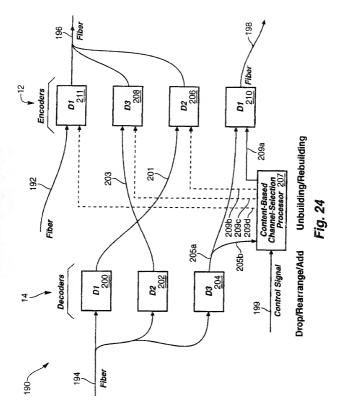
Electronic Processor Fig. 23A

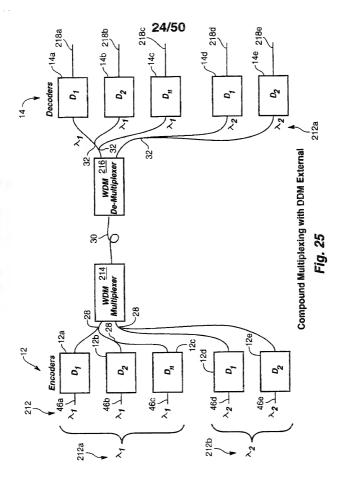


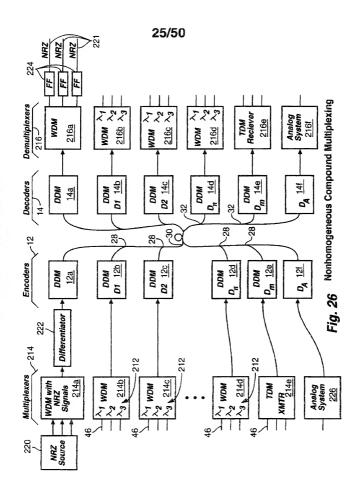


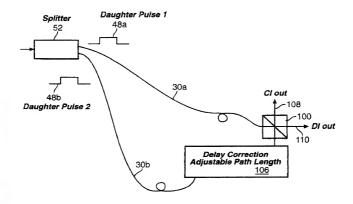
**Electronic Processor** 

Fig. 23B







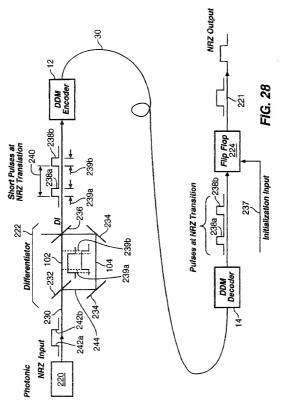


**Multiple Delay Path** 

Integrated Delay and Delay Correction

FIG. 27

Photonic NRZ Interface



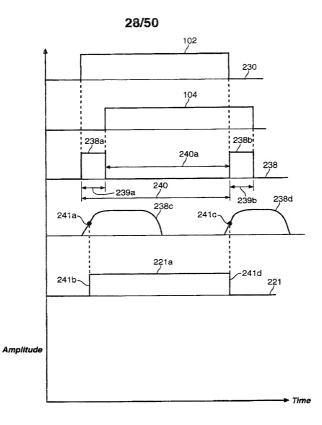
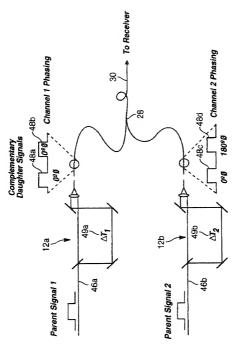


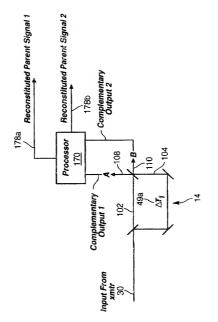
FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

Phase Sequenced Dual Channel Decoder



### **Phase Sequence Timing**

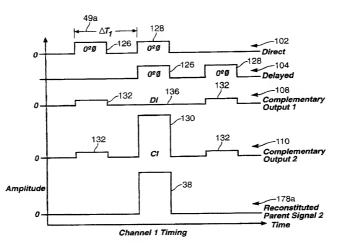


FIG. 32

## **Phase Sequence Timing**

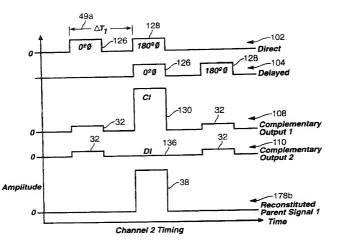
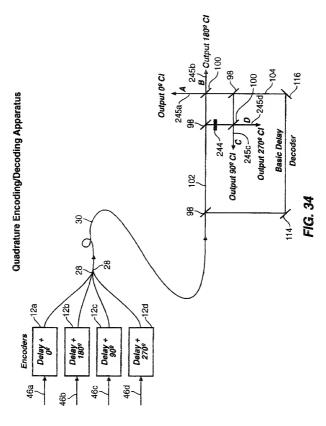


FIG. 33



	Phase of Direct Signal	Phase of Delayed Signal	Quadrature Outputs		
46a			A	В	C D
Channel 1	0	0	CI	DI	C = D
Channel 2	o	180	DI	CI	C = D
Channel 3	0	90	A =	B	CI DI
Channel 4	О	270	A =	B	DI CI
			1	<b>†</b>	<b>† †</b>
			245a	245b	245c 245d

FIG. 35

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#### Quadrature Wave Forms For One Channel

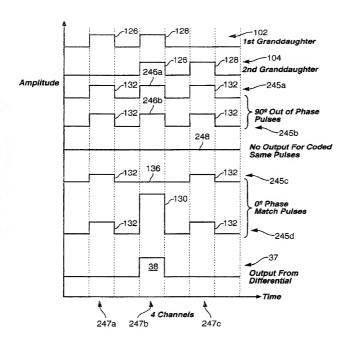


FIG. 36

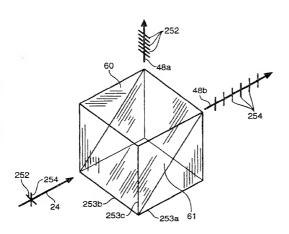


FIG. 37A

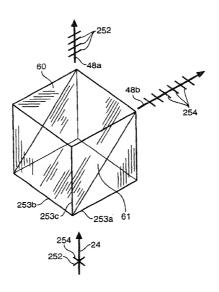
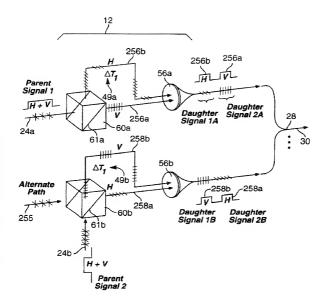
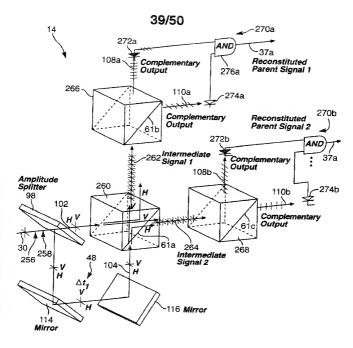


FIG. 37B

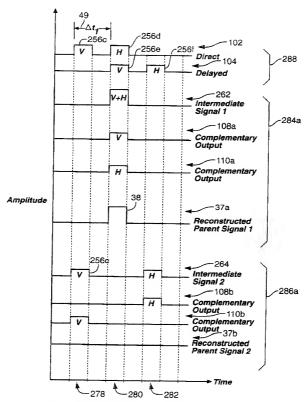
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Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Double Decoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Polarization Sequenced Channel 1 Timing

FIG. 40

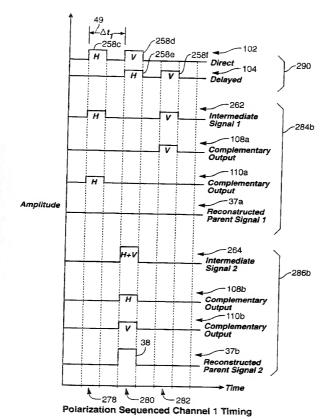


FIG. 41

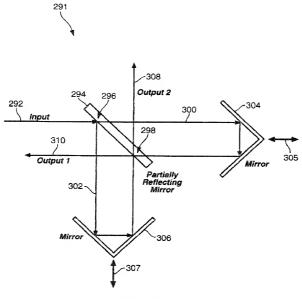


FIG. 42

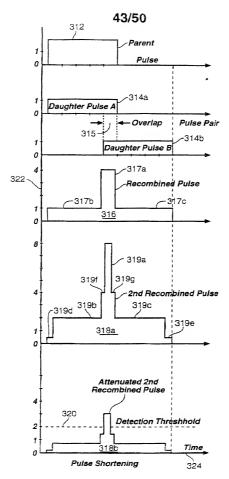


FIG. 43

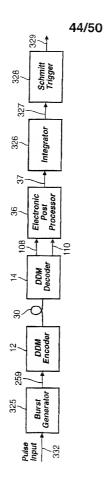


FIG. 44

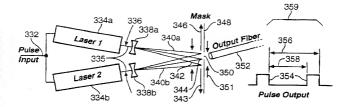


FIG. 45

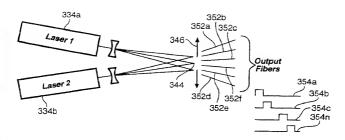


FIG. 46

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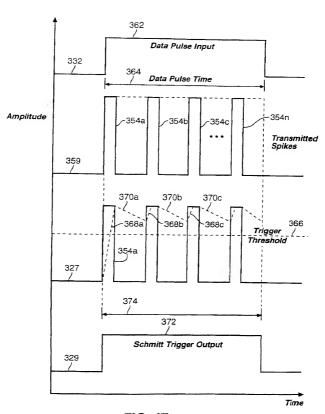


FIG. 47

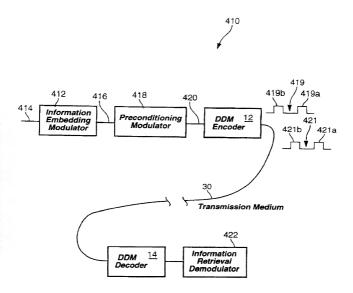


FIG. 48

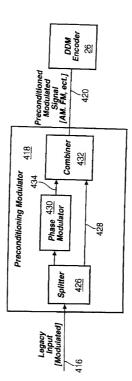


FIG. 49

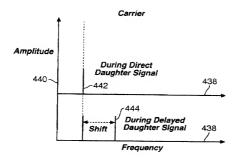


FIG. 50